I CLAIM:

1. A display apparatus comprising:

a display module; and

a power control unit coupled electrically to said display module, said power control unit including

an alternating current-to-direct current converter adapted to be connected electrically to an external power source so as to receive an alternating current power therefrom, said converter providing a direct current output,

a regulator connected electrically to said alternating current-to-direct current converter and having a power input end for receiving the direct current output from said alternating current-to-direct current converter, a control input end, and an output end, said regulator being operable in one of an enabled state, where said regulator outputs a target direct current power at said output end when said control input end receives a first level signal, and a disabled state, where said regulator does not output the target direct current power at said output end when said control input end receives a second level signal,

a delay circuit connected electrically to said alternating current-to-direct current converter and said control input end of said regulator, said delay circuit being capable of outputting one of the first and second level signals to said regulator,

a processor connected electrically to said output end of said regulator, said delay circuit and said display module, and

an electronic switch connected electrically to said delay circuit and said processor, said electronic switch being operable for switching from an OFF-mode, where said processor permits said delay circuit to output the second level signal to said regulator such that said regulator is operated in the disabled state, to an ON-mode, where said electronic switch initially enables said delay circuit to output the first level signal to said control input end of said regulator such that said processor receives the target direct current power from said regulator and where said electronic switch outputs a trigger signal to said processor so as to enable said processor to latch the first level signal outputted by said delay circuit and to provide the target direct current power to said display module.

2. The display apparatus as claimed in Claim 1, wherein the target direct current power has a voltage amplitude less than that of the direct current output.

3. The display apparatus as claimed in Claim 1, wherein said regulator includes a transistor that has a source serving as said power input end, and a gate serving as said control input end.

4. The display apparatus as claimed in Claim 1, wherein said processor defines a flag to indicate whether said

electronic switch is in the ON-mode or the OFF-mode.

5. The display apparatus as claimed in Claim 4, further comprising a non-volatile memory for storing the flag.

6. The display apparatus as claimed in Claim 5, wherein said processor permits said delay circuit to output the second level signal when the flag stored in said memory indicates that said electronic switch is in the OFF-mode, and to output the first level signal when the flag stored in said memory indicates that said electronic switch is in the ON-mode.

7. The display apparatus as claimed in Claim 1, wherein said processor includes an input/output port connected electrically to said delay circuit.

8. The display apparatus as claimed in Claim 7, wherein said delay circuit includes a resistor having one end connected electrically to said power input end of said regulator, and the other end connected electrically to said control input end of said regulator, and a capacitor having a first terminal connected electrically to the other end of said resistor, said control input end of said regulator and said input/output port of said processor, and a grounded second terminal.